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(58) Field of Search
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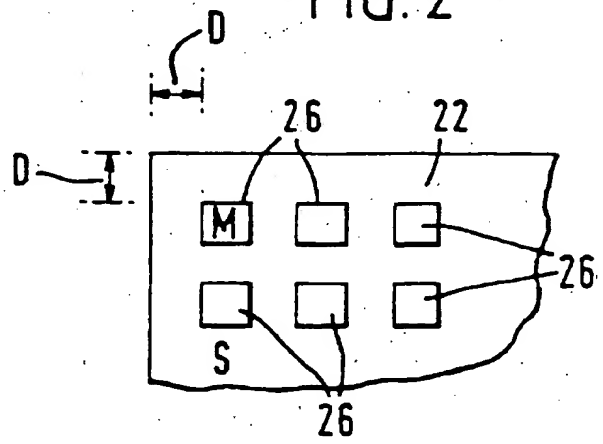
INT CL[6] G01T 1/24 , H01L
Online:WPI,JAPIO,INSPEC,EDOC

(54) Imaging detector and method of production

(57) In a semi conductor imaging detector, the distance D between the edge of the substrate (22) and the edgemost charge collection contact (26) is made as small as possible, preferably less than 500μm and/or less than 1/3 of the substrate thickness. Additionally or alternatively, a passivation layer (32, figure 5) between the edgemost portion of the contact and the substrate surface and/or a field shaping conductor adjacent to the surface. A field shaping region (36, figure 6) may also be arranged outside the edge of the substrate and may encircle each detector device, or it may encircle an arrangement of several devices. In such an arrangement, the spacing between adjacent detectors should be less than 500μm. A shield (50, figure 13) may also be used to shield the edge of each detector, or the edge region of the arrangement of several detectors, from incident radiation. Such arrangements can reduce the effect of edge image deterioration caused by strong field non-uniformities at the detector edges.

FIG. 2



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FIG. 1

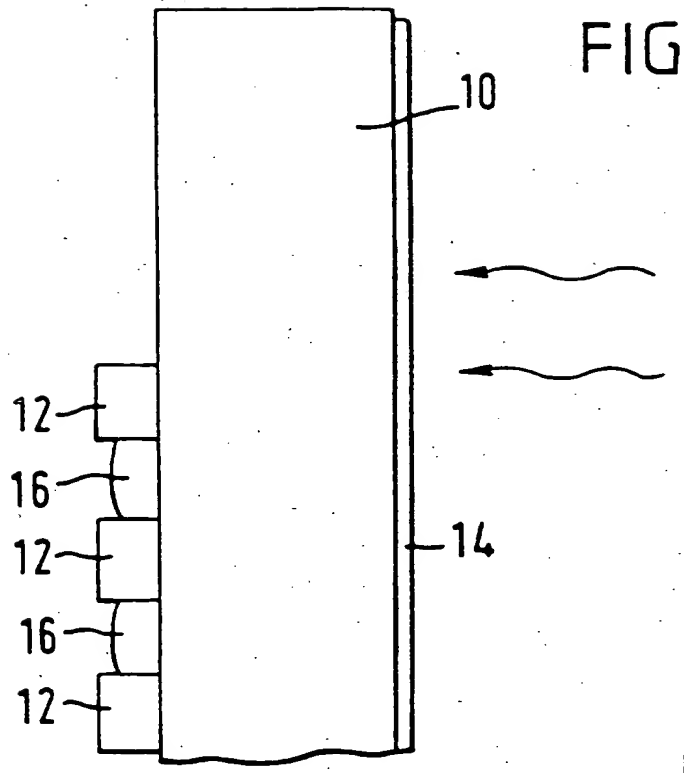


FIG. 2

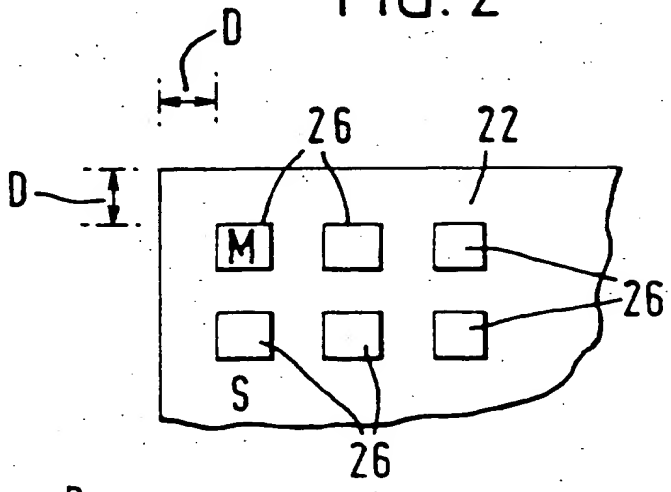


FIG. 3

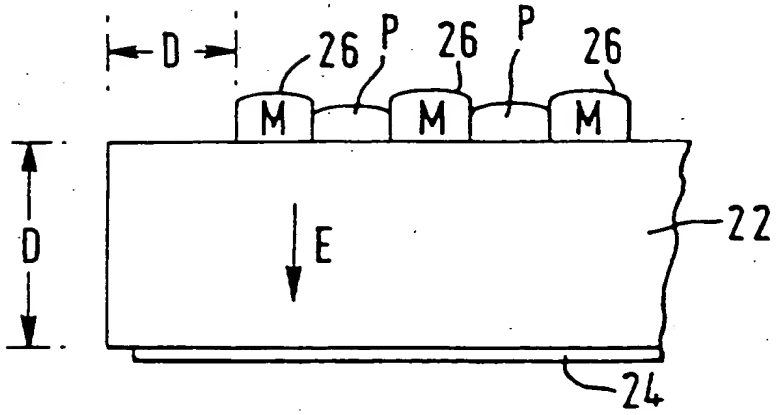
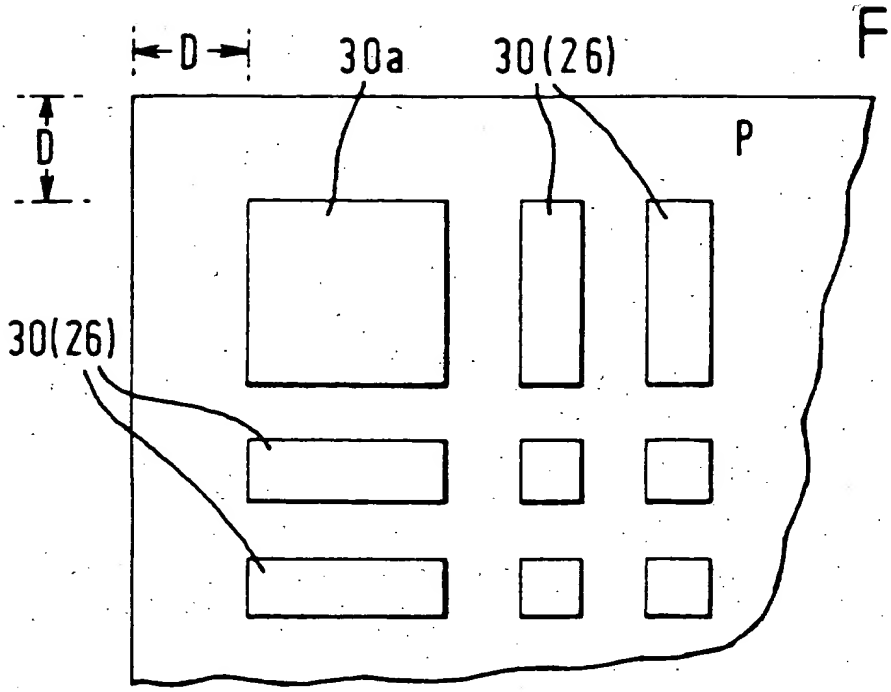


FIG. 4



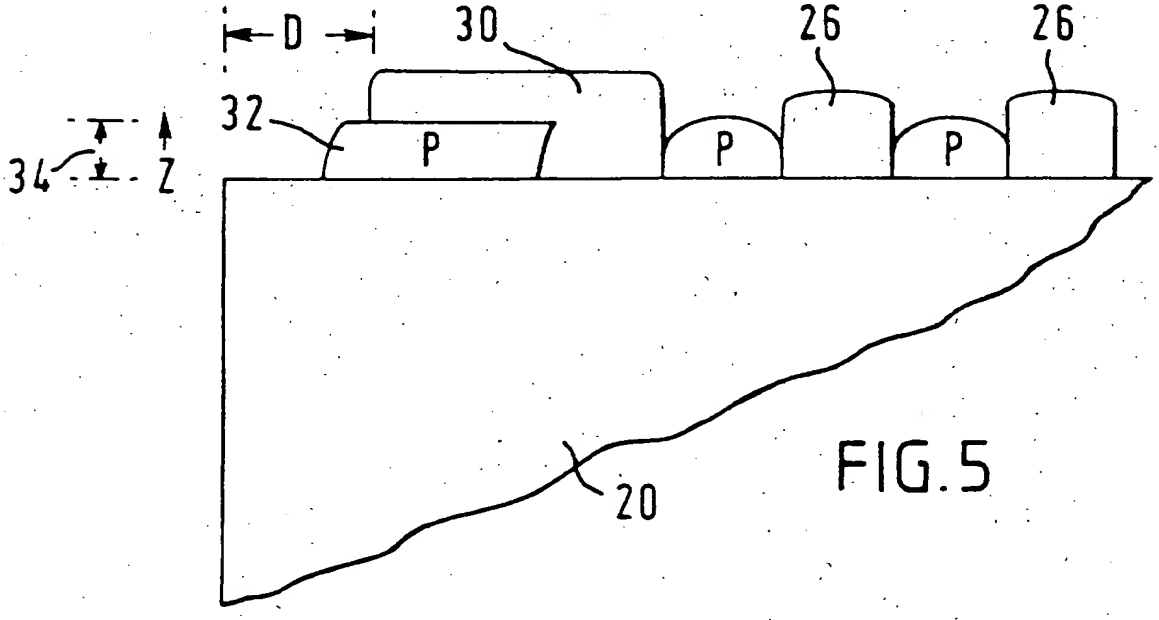


FIG.5

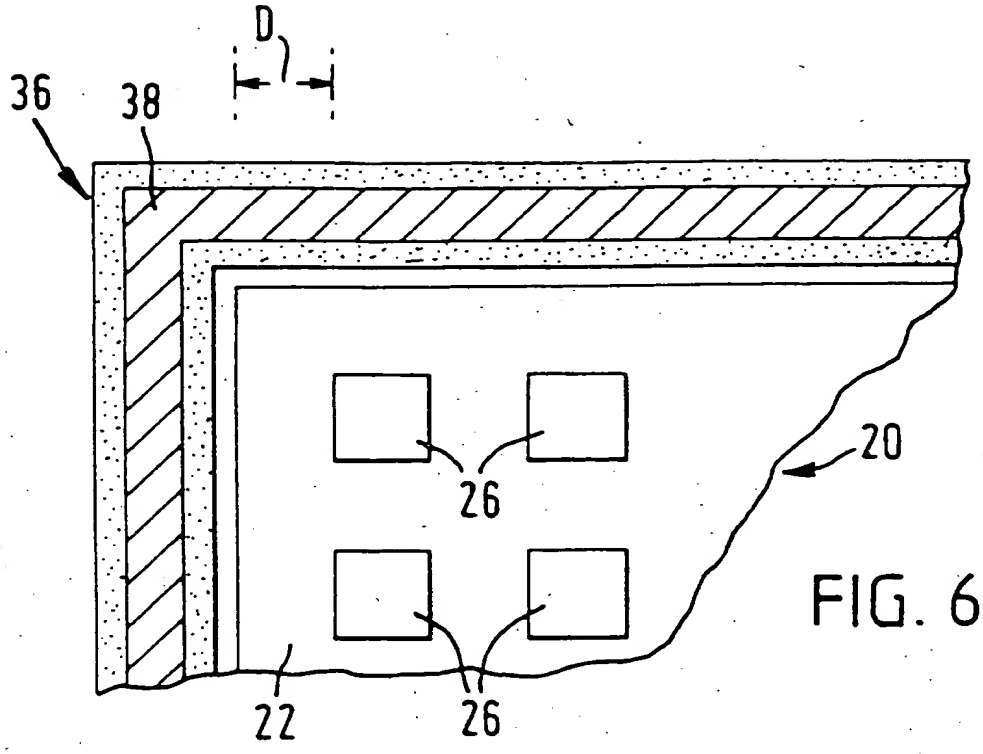


FIG. 6

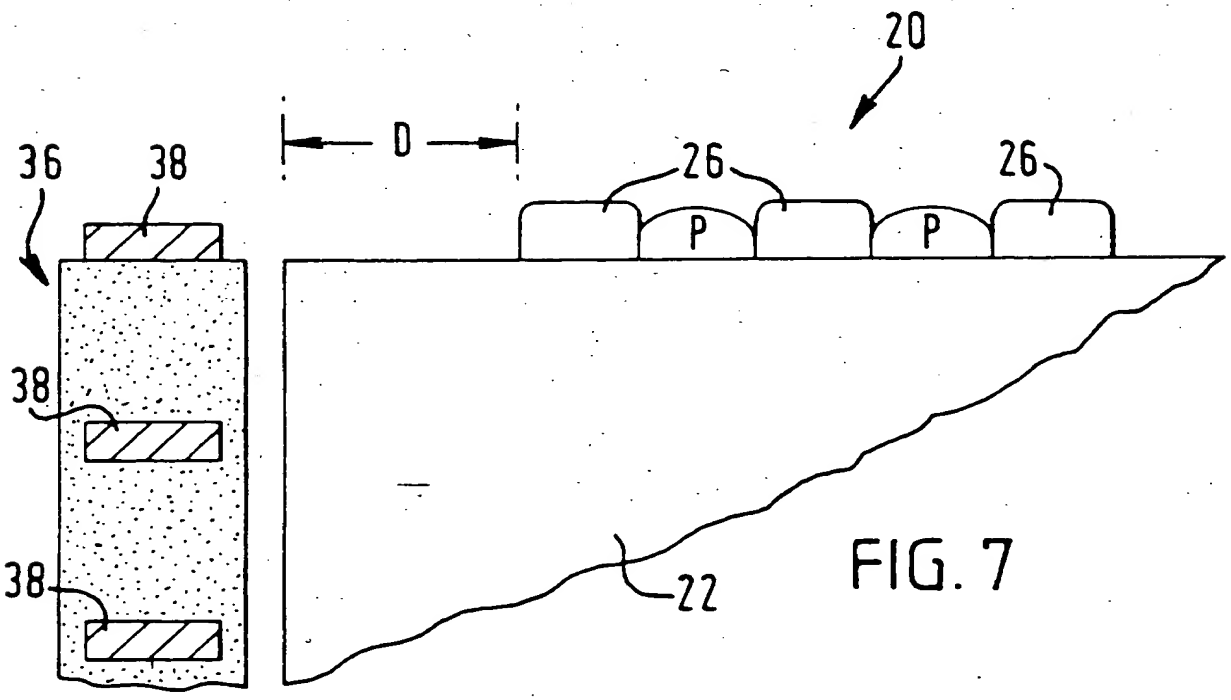


FIG. 7

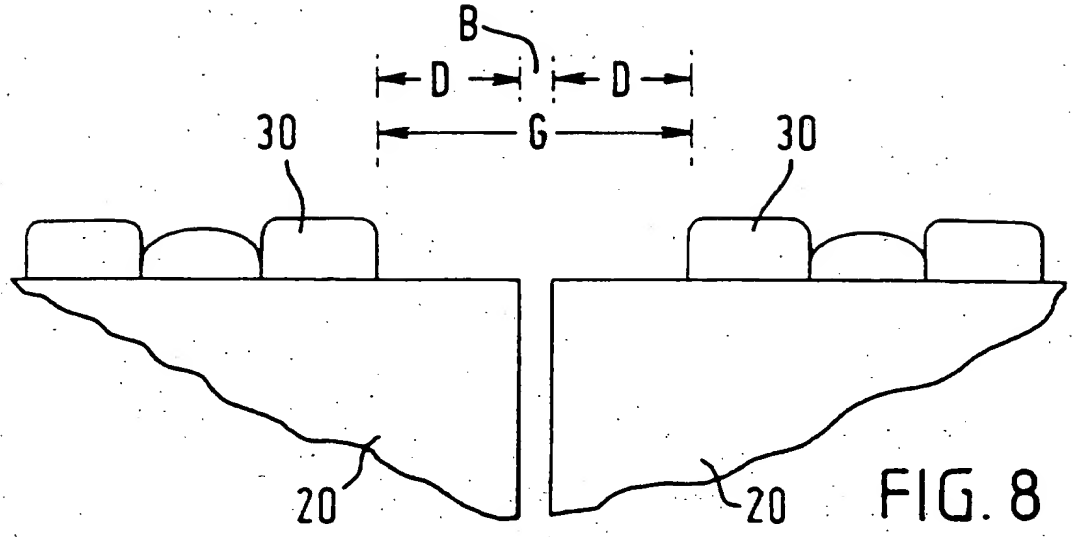


FIG. 8

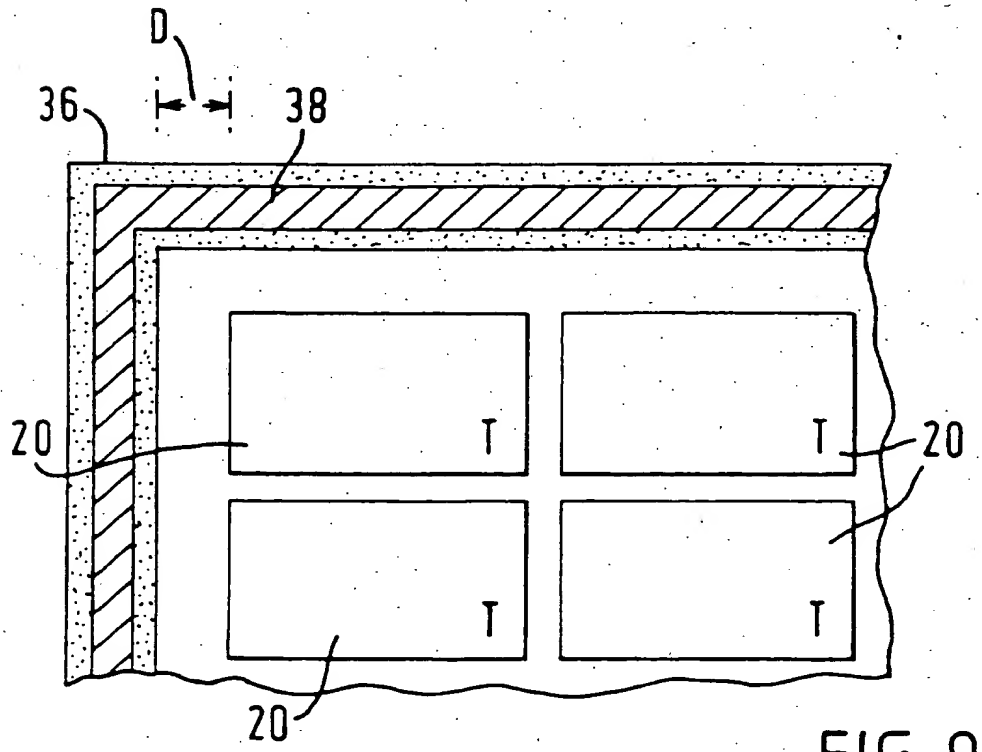


FIG. 9

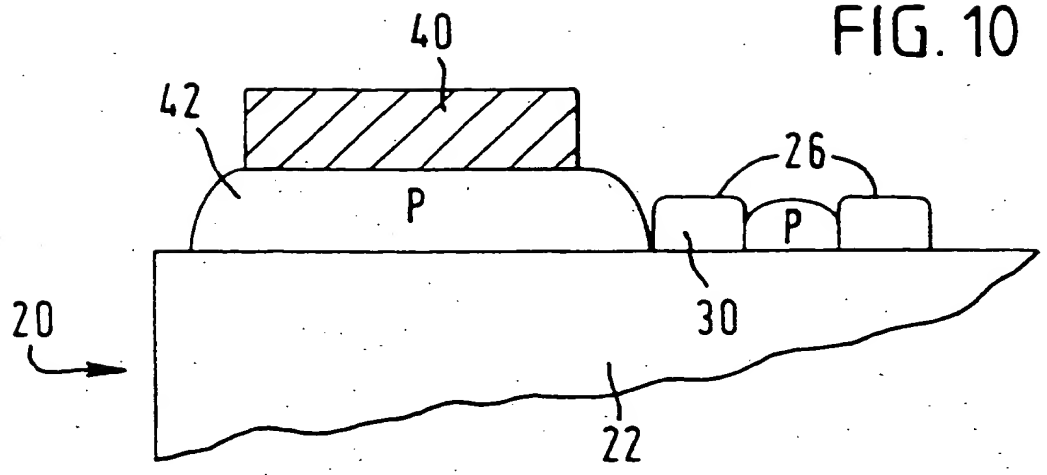


FIG. 10

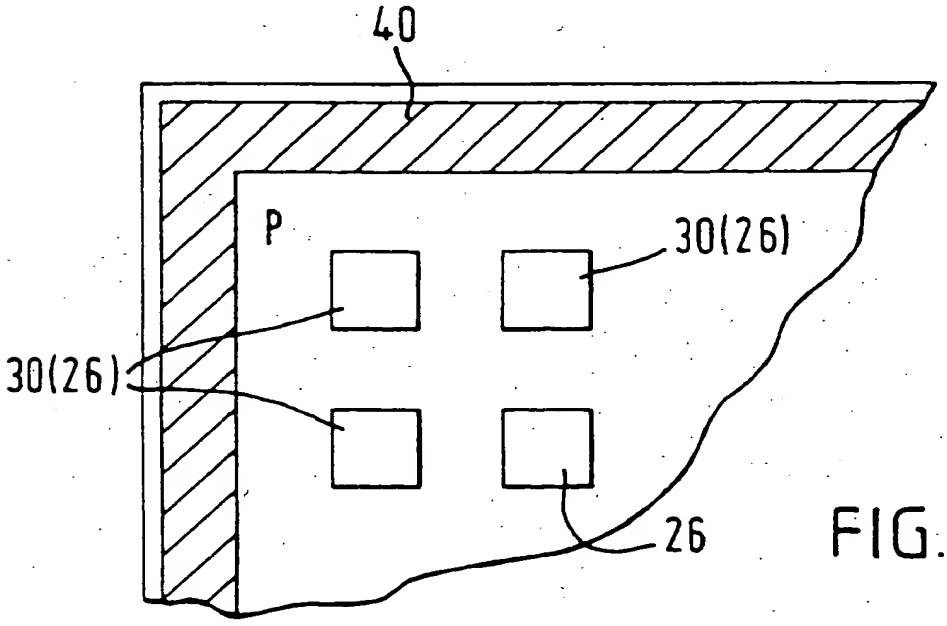


FIG. 11

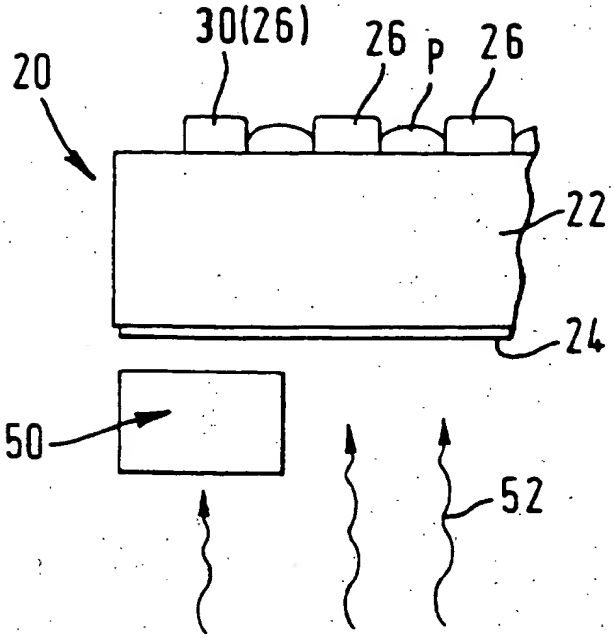


FIG. 12

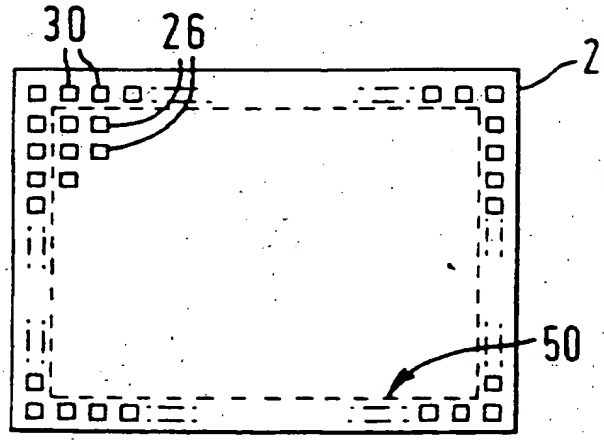


FIG. 13

IMAGING DETECTOR AND METHOD OF PRODUCTION

The present invention is directed to an imaging semiconductor device and to a method of producing such a device. In one form, the device is suitable for use in X-ray radiography, but the invention is not limited to this field. Typical devices comprise semiconductor material such as cadmium telluride (CdTe), cadmium zinc telluride (CdZnTe), mercury iodide (HgI_2), indium antimonide (InSb), gallium arsenide (GaAs), geranium (Ge), titanium bromide (TiBr), lead iodide (PbI) and silicon (Si), but, again, the invention is not limited to these materials.

An example of an imaging pixel semiconductor system is disclosed in published International Patent Application WO-A-95/33332 owned by the present assignee. The contents of this document are incorporated herein by reference.

Prior art silicon based semiconductor imaging devices have been implemented with a continuous grounded metal guard ring or pattern in electrical contact with the semiconductor material and encompassing the pixel contacts. The guard ring is formed on the sensitive face of the semiconductor material in the pixel plane adjacent to the edge of the material. The guard ring can improve electric field uniformity at the edge of the material which might otherwise cause image deterioration.

However, the guard ring occupies a significant area of the sensitive surface, creating a substantial "inactive" area around the periphery of the detector face. The region is inactive in the sense that it is impossible to detect photons incident in this region; any charge created by absorption of photons flows immediately to ground via the grounded guard ring. Typically, the pixel pitch might be as small as 35 μm, and the width of the guard ring might be at least as big if not significantly bigger (typically the width is in the range 25-500 μm).

The inactive area causes particular problems when several individual detectors are used together to form a tiled detector surface. The combined effect of the guard rings of adjacent tiles can create a blind area of 1 mm or more in width, at the region of the tile edges. Such a blind area is unacceptable for high sensitivity or high resolution imaging.

The present invention has been devised bearing these problems in mind. Various aspects of the present invention have arisen out of new development work carried out as described below, and as a result of appreciating problems not addressed hitherto.

In developing the present invention, an implementation of a detector system was tested using CdZnTe as the semiconductor material. CdZnTe is a desirable material (and may be preferred to Si) due to its high absorption efficiency for photon energies up to 90 keV. A high absorption efficiency is advantageous, because it means that X-ray images can be produced using lower doses of radiation.

Monolithic CdZnTe detectors (illustrated schematically in Figure 1) having an imaging area of 15 X 7mm^2 and a thickness t of about 1.5 mm were tested with X-ray energies from 20 to 100 KeV. In the detectors of Fig. 1, charge collecting (pixel) metal contacts 12 are arranged on one face of the detector material 10. The opposite face, the backplane, is covered with a continuous metal contact 14 extending to the detector edge. Incident radiation 16 enters the detector through the backplane. It will be appreciated that, in Fig. 1, all relative dimensions are arbitrary and the figure is not drawn to scale. The pixel pitch is 35μm, and the pixel metal contacts 12 start at from 0.6 to 1.6mm from the detector edge. A passivation layer 16 is introduced between adjacent pixel contacts to prevent crosstalk.

Before each image acquisition cycle, the pixel contacts 12 were reset to 5 V and the backplane 14 (the plane of incident radiation) was kept at a bias voltage Vb = 350 V.

During the development tests, images were taken of standard test objects with X-ray tube voltages ranging from 40 to 110 kV. The tube voltage defines the maximal photon energy incident on the detector.

Image deterioration was observed for tube voltages over 60 kV. The observed image deterioration commenced at the detector edges, and the extent of deterioration was observed to increase with increasing X-ray tube voltage. The deterioration was observed to consist of a white-out of the output signals from the edge of the detector, indicative of overloading or swamping of the detector signals. The deterioration was observed to be worst at pixels near the detector edges, becoming progressively better away from the edges. In what follows this effect is referred to as the Image Deterioration Effect (IDE).

As part of the tests, a frame was introduced to shield the edge regions of the detector from incident radiation. This significantly improved image quality.

During the development tests of this invention, it was concluded that the occurrence of this IDE at high energies might be caused by high energy photons interacting with the

semiconductor material near the pixel plane (i.e. metal contact plane). Furthermore, the occurrence of the IDE near the detector edges might be associated with the electric field non-uniformities near the outermost contact pixel edges.

In effect, the detector system may be considered as a parallel plate capacitor, the backplane conductor 14 forming one plate, and the pixel contacts 12 forming the other plate. The fringe field near the capacitor edges causes the electric field strength to be several times higher in magnitude near the edge compared to its uniform value elsewhere. Moreover, the electric field vector in the region of the non-uniformity has a high component along the direction parallel to the plane of the pixel contacts (the xy plane in Fig. 1). It is believed that IDE is caused by high energy photons reaching these high field regions, which causes an avalanche charge to be created in the region of the edgemost pixel contacts. The signal produced from the pixel contact is far in excess of the usual pixel signal level, and overloads the electronic circuitry for reading the signal.

The detector backplane 14 was covered completely by a gold layer of thickness 0.22μm. The continued occurrence of the IDE at higher photon energies supports the above hypothesis that the IDE is not caused by the backplane metallization edges.

Further evidence supporting the above developed hypothesis is provided by observation of the detector system behaviour at lower bias voltages: application of V_b = 100 V at the backplane electrode 14 eliminated the edge IDE problem despite causing a general deterioration of image contrast as a result of lower charge collection efficiency and higher charge diffusion.

One aspect of the present invention has resulted from the discovery that, if the edgemost contact element or elements on the surface of the semiconductor material is or are sufficiently close to the edge of the material, edge deterioration effects can at least be reduced, or even avoided nearly altogether.

A first aspect of the invention, therefore is that the distance between the edge of at least one charge collecting contact of a semiconductor imaging device, and the edge of the semiconductor material, be between 0 and about 500 μm and/or be between 0 and a value not significantly greater than 1/3 of the thickness of the semiconductor material.

By arranging at least some of the edgemost contacts close to the edge of the

semiconductor material, it is believed that the field non–uniformities are displaced closer to the edge of the semiconductor material and, if the spacing is sufficiently small, extend at least partly beyond (i.e. outside) the semiconductor volume. It will be appreciated that a reduction in the size of the semiconductor region affected by the non–uniformities will achieve a corresponding reduction in IDE at the edge of the detector.

The spacing between the edge of the semiconductor material and the outermost edge or edges of the or each pixel contact should preferably be sufficiently small to reduce, or alleviate, IDE in the detector, in use. Generally, best results are achieved if the spacing is made as small as possible.

With the knowledge of the present invention, the spacing for a particular semiconductor detector can be found by routine investigation, for example, either by routine experiment, or by simulation of the electrostatic fields as hypothesised above.

In one form, with increasing preference for smaller fractions, it is preferred that the spacing be not significantly greater than about 1/5, or about 1/15, or about 1/30, or about 1/50, of the semiconductor thickness. Such ratios of spacing/thickness can provide increasingly better results in alleviating edge IDE.

In another form, with increasing preference for smaller values, it is preferred that the edge spacing be not significantly greater than about 300 μm, or 100 μm, or 50 μm or 30μm. These values match the above fractions for a semiconductor thickness of 1.5 mm, but can also be applied irrespective of the semiconductor thickness in other cases.

Selected ones of the above values may also be combined to give a preferred spacing of not significantly greater than about 1/3 (or 1/5, etc.) of the semiconductor thickness if greater than 1.5 mm, and not significantly greater than about 500 μm (or 300 μm, etc.) if the semiconductor thickness is generally equal to or less than 1.5 mm.

Various methods can be used to produce a semiconductor imaging device with an edge spacing as defined above.

According to another aspect of the invention, one suitable method is to form the contact(s) on the surface of a pre–cut (or pre–formed) semiconductor substrate of the desired size, using photolithography. Modern photolithographic techniques can be used to form a contact within about 50μm of the substrate edge.

According to another aspect of the invention, an alternative technique is to form the contact(s) on the surface of an oversized substrate using any convenient technique, and to cut the edge of the substrate close to the edgemost contact(s). Modern cutting techniques can be used to form a cut to a precision of about 10μm, or better.

In a closely related aspect, an edgemost portion of at least one charge collecting contact of a semiconductor imaging device is spaced from the surface of the semiconductor material by passivation material.

For example, the edgemost contacts may have a step profile (or at least the side of the contact adjacent to the semiconductor material may have a step profile) and be arranged so that the portion which steps away from the surface of the semiconductor substrate extends towards the edge of the semiconductor substrate.

This takes into account that the strong field non-uniformities are believed only to exist in the semiconductor material very close to the surface on which the charge collection contacts are mounted. By spacing the edgemost portion of the contact from the semiconductor surface, and introducing a passivation layer, the most intense field is confined to the non-sensitive passivation material, where no breakdown effect is possible.

This technique can be particularly effective when used in combination with the previous technique of positioning the edgemost charge collection contact(s) close to the edge of the semiconductor material.

In another closely related aspect, a non-sensitive field shaping region is arranged outside, but adjacent to, at least one edge of the semiconductor imaging device.

Such an arrangement can avoid reducing the area on which charge collection contacts can be mounted (which is a deficiency of using a guard ring), yet still provide a field shaping, or controlling effect to reduce edge IDE problems.

For example, the field shaping region may comprise non-sensitive material within which is or are arranged one or more field shaping strips. The positions of the strips, and the potential(s) applied to the strips can be chosen to achieve the desired field shaping. Different potentials can be applied to different strips if desired.

The field shaping region may extend around the periphery of each single detector element. Additionally, or alternatively, the field shaping region may extend around the

external periphery of a detector made up of a number of separate detector units (e.g. tiles) positioned side by side.

A further aspect of the present invention is to arrange two or more detector units in very close proximity with each other, or in direct contact with each other. Typically, the detectors may be arranged with a gap of not significantly more than 500 μm. With increasing preference for smaller gaps, the spacing is more preferably not significantly greater than about 300 μm, or about 100 μm, or about 50 μm or less (which is equivalent to direct contact). With such close "spacing", the strong edge field non-uniformities of one detector may at least partially cancel out the corresponding edge non-uniformities of an adjacent detector, and thereby reduce the likelihood of edge IDE.

This proximity of neighbouring tiles on an imaging support plane is feasible with existing positioning and aligning methods.

This technique may be most effective when used in combination with the technique of positioning the edgemost charge collection contact(s) very close to the edge of the semiconductor material and/or in combination with the technique of using passivation between an edgemost portion of a contact and the semiconductor material.

A further aspect of the invention is to define on the radiation receiving surface of a semiconductor imaging device, or of an arrangement of several devices, a window region (smaller than the overall surface of the device or devices) for receiving incident radiation. In other words, one or more regions of the surface are shielded from receiving incident radiation.

With such a technique, incident radiation can be confined to a region of the semiconductor material where strong field non-uniformities are absent. Preferably, at least one edge region of the substrate is shielded to prevent charge being produced in the edge region vulnerable to IDE. One feature of IDE is that, once a charge avalanche has started, the avalanche affects not only the closest charge collecting contact, but spreads to affect other contacts in the vicinity. By reducing the "window" of the detector even by a modest amount to reduce the amount of incident radiation in regions of strong field non-uniformity and thereby suppress IDE, it is believed that a significant improvement can be achieved.In one form, the window region may correspond to the area in alignment with the charge collecting contacts formed on the opposite surface of the semiconductor material.

Alternatively, the window region may be slightly smaller than this, so that some of the edgemost contacts are in the shielded region.

In another aspect of the invention, at least a portion of a field shaping conductor adjacent to the surface of the semiconductor material of a semiconductor imaging device is spaced from the surface by passivation material. Preferably, the conductor is insulated electrically from the semiconductive material by the passivation material. Therefore, in contrast to the prior art, a field shaping, or "guard", conductor should not make electrical contact with the surface of the semiconductor material. By electrically isolating the field shaping conductor from the semiconductor material, charge created by incident photons cannot flow out through the conductor. Instead, the charge is available to flow towards an adjacent charge collection contact, as a detectable output.

The proximity of the conductor to the semiconductor material nevertheless enables it to provide a field shaping, or "guard", effect to reduce field non–uniformities at the edge of the semiconductor material. The conductor may be coupled to ground, or to some other potential, for this purpose.

With the above arrangement using the field shaping conductor, the sensitivity of the detector in the edge regions can thus be improved, but the presence of the guard ring limits the resolution in the edge region of the detector. It is preferred that the width of the guard conductor on the semiconductor surface be not significantly greater than about 100 μm, so that it does not occupy too much surface area. With a guard conductor of this width, the "hole" in the resolution at the detector edge is also about 100 μm.

The above aspects may be used independently, or two or more aspects may be used advantageously in combination. In contrast to the teaching of the prior art, the above aspects can enable incident radiation to be detected in the peripheral region of the semiconductive material. This provides an extremely important advantage in improving the sensitivity of the detector in the edge regions, and can enable the size of "dead" or "blind" regions of the detector to be reduced compared to currently known devices. With the invention, two or more detectors can be arranged in a one–, two– or three–dimensional pattern (such as a tiled detector surface) and can provide a much more uniform sensitivity across the entire width of the detection surface.

In its various aspects, the invention can reduce or even alleviate field non-uniformities at the edge of the detector sensitive area while, at the same time, achieving a sensitive area which is maximal and substantially equal to the total area of the detector.

Embodiments of the invention are now described by way of example, with reference to the following further drawings, in which:-

Fig. 2 is a schematic plan view of one corner of pixel surface of a semiconductive substrate of a first embodiment;

Fig. 3 is a schematic side view of the detector region illustrated in Fig. 1;

Fig. 4 is a schematic plan view showing a modified second embodiment;

Fig. 5 is a schematic side view of a modified third embodiment;

Fig. 6 is a schematic plan view of a modified fourth embodiment;

Fig. 7 is a schematic side view of the region of Fig. 6;

Fig. 8 is a schematic side view of a plurality of detector tiles in a modified fifth embodiment;

Fig. 9 is a schematic plan view of the plurality of detector tiles in a modified sixth embodiment;

Fig. 10 is a schematic plan view of a modified seventh embodiment of semiconductor imaging device;

Fig. 11 is a schematic side view of the region of the detector shown in Fig. 10.

Fig. 12 is a schematic side view of a region of a modified eighth embodiment employing a shield; and

Fig. 13 is a schematic plan view of the detector of Fig. 12.

Referring to Figs. 2 and 3, a semiconductor X-ray imaging device 20 includes a semiconductor substrate 22 on one face of which is formed a backplane conductive layer 24, and on the other face of which are formed a plurality of metal contacts 26. The detector operates in a similar manner to that described in the above referenced International application No. WO-A-95/33332, and so the basic operation need not be described further here. The contacts 26 act as charge collection contacts through which electronic circuitry (not shown) can read out charge signals generated by the absorption of X-ray radiation incident through the backplane 24.

This embodiment takes advantage of the observation in accordance with one aspect of the invention that the Image Deterioration Effect (IDE) does not occur near the backplane where the entire detector area is covered with a continuous metal layer extending to the detector edge. In this embodiment, the distance D between the substrate edge and the outermost cell metal contacts at the cell contact plane are sufficiently small (and preferably minimised within practical limits) that IDE can be avoided in the pixel plane.

As the distance D is lowered, the non-uniformities in the edge electric field are believed to be pushed near the detector edge and eventually extend partially beyond the detector volume. There is believed to be a correlation between the detector thickness and the electric field non-uniformity: the thinner the detector, the higher the non-uniformity, and therefore, the smaller the desirable distance D. In this particular embodiment, with a 1.5mm thick detector, the effect of field non-uniformities begins to moderate when the distance D becomes lower than 500-300 μm. More preferably, this effect becomes less significant if the distance D becomes lower than 100 μm and even more preferably, this effect becomes even less significant if the distance D becomes 30 μm or lower. Although the drawings illustrate a detector which is generally symmetrical in two dimensions, it will be appreciated that this is not essential. For example in Fig. 2, the horizontal distance D need not necessarily be the same as the vertical distance D. Furthermore, the corresponding distances D at the opposite edges of the detector need not be the same.

The shape of the metal contacts is not necessarily square, as shown in Figure 2, but can take any shape, for example, circular, parallelogram (strip-like) polygonal, etc. Furthermore, the shapes and sizes of contacts of different cells are not necessarily identical to one another (see, for example, the arrangement in Fig. 4). In Fig. 4, the outermost rows and columns of contacts 30 are shaped so that they extend towards the detector edge or edges. The corner metal contact 30a is larger in order to keep the edge distance D small.

These embodiments of detector may typically be produced in two possible ways. The first way is to form directly as many metal contacts as needed in position relative to an edge of the substrate, to achieve the desirable minimal or sufficiently small distance D. In this way of implementing the invention, the minimum achieved distance D is limited only by the accuracy of the particular photolithography technique used. With conventional

photolithography techniques, charge collecting metal contacts can be implemented as close as 50 μm from the detector edge (for CdTe or CdZnTe).

The alternative second way of producing a detector in accordance with these embodiments is to form the metal contacts on a substrate of larger dimensions than ultimately needed, and to remove excess semiconductive material from at least one edge (for example, by cutting). The precision of modern cutting techniques (for example, diamond cutting) is around 10–20 μm.

A particular advantage achieved by the embodiments of Figs. 2 to 4 is that the edge region of the semiconductive material is actively sensitive (in that incident photons can be detected even close to the edge). The proximity of the metal contacts to the edge of the substrate helps reduce IDE at the detector edge. Moreover, the proximity of the metal contacts to the substrate edge means that image resolution is not sacrificed in the edge region. A plurality of such detectors may be used side by side, for example, to produce a tiled imaging detector surface. Such a surface would have more uniform sensitivity, resolution than that achievable hitherto.

Referring To Fig. 5, another embodiment of the invention uses a passivation layer 32 under a portion of the edgemost metal contacts 30. With such a passivation layer, the largest part of the field non-uniformity will extend in a non-sensitive medium such as the passivation. For example, the thickness 34 of the passivation layer can be several μm thick. This embodiment, takes into account the fact that the field nonuniformities increase with decreasing magnitude of distance z to the metal contacts 30. Although not essential, this embodiment also uses a "minimum" or at least sufficiently small edge distance D, to reduce the intensity of the field non-uniformities at the edge. Such a combination can confine the most intense electric field in a non-sensitive medium such as outside the semiconductive material, and/or in the edge passivation 32 where no breakdown effect is possible.

Referring to Figs. 6 and 7, in another embodiment of the invention, the semiconductor substrate 22 is surrounded with a non-detecting field shaping region 36, which lies outside, but closely adjacent to, the substrate. The region 36 may contain any number of field shaping metal strips 38, and one or more voltages can be applied to the strips. The voltages for the different field shaping strips 38 can be different from one another and are suitably chosen so

as to achieve the desired field shaping. It is to be noted that the dimensions illustrated in Figs. 6 and 7 are arbitrary. Furthermore, this embodiment of the invention (field shaping) can be used in conjunction with the other embodiments already described (extended edge metal contact, extended edge metal contact over a passivation layer).

In a further embodiment, the minimization of the edge distance D as defined previously, can be used to remove field non-uniformities for a large area imaging area system comprising several monolithic detectors (tiles). Referring to Fig. 8, different detector tiles 20, each with a minimal edge distance D are placed side by side(the number of tiles and dimensions in this figure being arbitrary and not limiting). Field non-uniformities near the edge metal contacts 30 of neighbouring tiles mutually cancel out a large extent. The gap G between the neighbouring edge metal contacts is G=2 X D+B where B is the gap between the substrates of neighbouring tiles. According to this embodiment of the invention, the distance B is also minimal. Preferably, this distance B is not greater than about 500-300 μm, more preferably, is not greater than around 100 μm and even more preferably B is 50 μm or less. This proximity of neighbouring imaging tiles on an imaging plane is feasible with existing positioning and aligning methods. This embodiment of the invention (juxtaposition of tiles) can be used in conjunction with the other embodiments already described (extended edge metal contact, extended edge metal contact over a passivation layer).

Referring to Fig. 9, in an alternative embodiment of the invention, the use of a field shaping structure comprising a nonsensitive medium 36 and field shaping strips 38 as described previously with reference to Figs. 6 and 7 can be used to minimise field non-uniformities at the edges of a multi-tile system. The field shaping structure surrounds the multi-tile system thus providing the necessary field shaping at the edges of the entire system. The dimensions and number of tiles in Figure 9 are arbitrary and not limiting.

Figs. 10 and 11 illustrate an alternative embodiment which employs a guard metal conductor, but which can nevertheless achieve an active region corresponding to substantially the entire volume of the semiconductor substrate 22. In this embodiment, a guard ring conductor 40 is spaced from the surface of the semiconductor substrate 22, and is electrically insulated therefrom, by means of a passivation layer 42. The guard ring can extend the metallization to practically the very edge of the semiconductor substrate, and thus reduce the

edge non-uniformities in the region of the edgemost contacts 30 which the guard conductor 40 surrounds. At the same time, since the guard ring 40 is not in electrical contact with the substrate 22, it does not sink any charges from the substrate. Any charge generated in the edge region of the substrate 22 by absorption of photons will drift towards the edgemost contacts 30, from which it can be collected as a useful signal. Thus, the substrate does not contain any inactive region, although the spatial resolution will be lower at the edges because the peripheral surface area is occupied by the guard ring 40 instead of by charge collecting contacts 30. For this reason, the width of the guard ring conductor 40 should not be too large. Typically it may be about 50-100 μm in width.

The voltage applied to the guard ring conductor 40 may be selected optimally so that each charge created by ionization below the guard ring will drift towards the nearest edge contact 30. For example, if the charge collection contacts are reset to about 5 volts, and a bias voltage of about -350 volts is applied to the backplane 24, then the potential applied to the guard ring conductor 40 may conveniently be 0 volts.

Referring to Figs. 12 and 13, in an alternative embodiment, a shield (a frame 50 in this example) may be used to shield vulnerable edge regions of the substrate 22 from receiving incident radiation. Radiation 52 incident within the window region defined by the frame 50 is allowed to pass into the substrate 22, whereas radiation 54 incident outside the window region is blocked by the frame 50. The shield may be made of any suitable material for preventing the transmission therethrough of the radiation of interest, for example, steel for shielding X-rays.

By shielding the edge regions, the amount of charge generated at the edge regions where the field non-uniformities are strongest, will be reduced. The effect of this is to suppress IDE, and to improve the image quality. As explained previously, the IDE has been observed to affect not only the outermost contacts, but any contacts in the same vicinity. Therefore, by suppressing IDE, image quality at the image edge and at regions inward of the edge can be significantly improved. This improvement can more than make up for the slight reduction in the size of the active area of the detector.

The shield may be arranged so that its inner edge is aligned outside the edgemost contacts 30, or it may be arranged so that it covers, or at least partly covers, one or more

rows or columns of edgemost contacts (as illustrated in Figs. 12 and 13).

The shielding frame 50 is preferably positioned either in contact with, or very close to, the backplane 24 of the detector.

Although a rectangular window defining frame 50 is illustrated, it will be appreciated that this is merely an example, and is not limiting. One or more continuous, or disparate, regions of the surface can be shielded as desired.

As a modification, instead of applying the shielding frame to an individual detector, a large frame may be positioned to shield the edge region of an extended detector array formed of a plurality of individual detectors positioned side by side (defining a tiled or mosaic detector surface). With such an arrangement, the frame could, for example, be arranged to shield the peripheral region of each edgemost detector in the array.

It will be appreciated that the shield is different from a collimator which may be used on a detector, because the shield in the above embodiments does not limit the angle of incidence of incoming radiation. Typically, it is desired only to shield the edgemost regions of the substrate surface which are vulnerable to strong field non-uniformities, and it is desired at the same time to provide a detector window which is as large as possible. Typically, the window would be several times bigger than a collimator aperture.

As illustrated by the above described embodiments, the invention can improve the sensitivity in the edge region of a semiconductor imaging device, giving the device a more uniform sensitivity throughout its volume, and avoiding the occurrence of inactive regions as in the prior art. Furthermore, embodiments of the invention can improve the detection resolution at the detector edges, and can avoid, or at least reduce the effect of, resolution "holes" at the device's edges, which is a particular problem in prior art devices.

Although the present invention has been described in relation to X-ray detection and is particularly suitable in this field, the invention can be used in many other applications, and is not intended to be limited only to the detection of X-rays.

Although the subject matter believed to be of particular importance has been defined in the description and in the appended claims, it is to be appreciated that the Applicant claims protection of all novel subject described herein, irrespective of whether particular emphasis has been placed thereon.

CLAIMS

1. A semiconductor imaging device comprising a substrate of semiconductive material, and at least one charge collection contact formed thereon, the distance between the charge collection contact and an edge of the substrate being between 0 and about 500μm and/or being between 0 and a value which is not significantly greater than about 1/3 of the thickness of the substrate.

2. A device according to claim 1, wherein said distance is between 0 and a value which is not significantly greater than about 1/5 of the substrate thickness.

3. A device according to claim 2, wherein said distance is between 0 and a value which is not significantly greater than about 1/15 of the substrate thickness.

4. A device according to claim 3, wherein said distance is between 0 and a value which is not significantly greater than about 1/30 of the substrate thickness.

5. A device according to claim 4, wherein said distance is between 0 and a value which is not significantly greater than about 1/50 of the substrate thickness.

6. A device according to any preceding claim, wherein said distance is between 0 and a value not significantly greater than about 300 μm.

7. A device according to claim 6, wherein said distance is between 0 and a value not significantly greater than about 100 μm.

8. A device according to claim 7, wherein said distance is between 0 and a value not significantly greater than about 50 μm.

9. A device according to claim 8, wherein said distance is between 0 and a value not

significantly greater than about 30 μm.

10. A semiconductor device according to any preceding claim, wherein an edgemost portion of the charge collection contact, and/or at least a portion of a field shaping conductor, is spaced from the surface of the semi conductor substrate by passivation material.

11. A semiconductor imaging device comprising a substrate of semiconductive material, and at least one charge collection contact formed thereon, wherein an edgemost portion of the charge collection contact, and/or at least a portion of a field shaping conductor, is spaced from the surface of the semiconductor substrate by passivation material.

12. A device according to claim 10 or 11, wherein the side of the contact adjacent to the semiconductive material is stepped away from the semiconductor surface.

13. A device according to claim 12, wherein the contact has generally a step profile.

14. A device according to claim 10, 11, 12 or 13, wherein the field shaping conductor is electrically insulated from the semiconductor substrate by the passivation material.

15. A device according to claim 10, 11, 12, 13 or 14, wherein field shaping conductor extends adjacent to an edge region of the substrate.

16. A device according to any of claims 10 to 15, further comprising means for applying a predetermined voltage to the field shaping conductor.

17. A device according to any preceding claim, further comprising an outer non-sensitive field shaping region arranged outside, and adjacent to at least one edge of, the semiconductor substrate.

18. A semiconductor imaging device comprising a substrate of semiconductive material,

at least one charge collection contact formed thereon, and an outer non-sensitive field shaping region arranged outside, and adjacent to at least one edge of, the semiconductor substrate.

19. A device according to claim 17 or 18, wherein the outer non-sensitive field shaping region comprises one or more conductors which are electrically isolated from the semiconductor substrate.

20. A device according to claim 19, further comprising means for applying a predetermined voltage to at least one of the conductors of the outer field shaping region.

21. A device according to claim 20, further comprising second means for applying a predetermined different voltage to at least one or more other conductors of the outer field shaping region.

22. A device according to claim 19, 20 or 21, wherein the one or more conductors are carried on, or in, a dielectric.

23. A device according to any preceding claim, and further comprising means for defining on a sensitive surface of the substrate, a predetermined window region for receiving incident radiation.

24. A semiconductor imaging device having a semiconductor substrate with a radiation sensitive surface, and means for defining on said surface a window region smaller than the surface area of the substrate, for receiving incident radiation.

25. A device according to claim 23 or 24, wherein the window defining means shields one or more regions of the semiconductor substrate from receiving incident radiation.

26. A device according to claim 25, wherein at least one shielded region corresponds to a portion of the substrate, subject, in use, to high electric field non-uniformities.

27. A device according to claim 25 or 26, wherein at least one shielded region is an edge region of the substrate.

28. A device according to claim 27, wherein the window defining means comprises a frame of material which is non-transparent to radiation to be detected.

29. A device according to any of claims 23 to 28, wherein the window defining means is positioned in contact with, or closely adjacent to, the radiation receiving surface of the semiconductor substrate.

30. A device according to any of claims 23 to 29, wherein the window defining means is made of steel.

31. An assembly comprising a plurality of semiconductor imaging devices arranged side by side to define an extended surface, and means for shielding one or more regions of the extended surface from receiving incident radiation, to define an imaging surface smaller than said extended surface.

32. An assembly comprising a plurality of semiconductor imaging devices arranged adjacent to each other to define an extended imaging surface, each device comprising a semiconductor substrate for receiving incident radiation, and the assembly further comprising an outer field shaping region positioned outside, but closely adjacent to an outer edge of, the extended imaging surface.

33. An assembly according to claim 32, wherein the field shaping region encompasses the edge or edges of the extended imaging surfaces defined by the plurality of imaging devices.

34. An assembly according to claim 32 or 33, wherein the field shaping region comprises one or more conductors which are electrically insulated from the adjacent imaging devices.

35. An assembly according to claim 31, 32, 33 or 34, wherein at least a first and a second of said imaging devices are positioned in edge to edge contact with each other, or with an edge to edge spacing of not significantly more than about 500μm

36. An assembly comprising first and second semiconductor imaging devices, each device comprising a semiconductor substrate on which is mounted at least one charge collection electrode for the device, the first and second devices being positioned side by side in edge to edge contact with each other, or with an edge to edge spacing of not significantly more than about 500 μm.

37. An assembly according to claim 35 or 36, wherein the edge to edge spacing is not significantly more than about 100μm.

38. An assembly according to claim 37, wherein the edge to edge spacing is not significantly more than about 50μm.

39. An assembly according to any claims 31 to 38, wherein at least one of the imaging devices is a device as defined in any claims 1 to 30.

40. An assembly according to any of claims 31 to 39, wherein the imaging devices define an elongated imaging surface.

41. An assembly according to any of claims 31 to 40, wherein the imaging devices define a two-dimensional mosaic imaging surface.

42. A method of producing a semiconductor imaging device as defined in any of claims 1 to 10, the method comprising preparing a said semiconductor substrate of a predetermined size for the imaging device, and forming a said at least one charge collecting contact on the substrate at said distance from an edge of the substrate using a lithographic process.

43. A method of producing a semiconductor imaging device as defined in any of claims 1 to 10, the method comprising forming a said at least one charge collecting contact on an oversize semiconductor substrate, and removing material from the substrate adjacent to at least one edge to achieve said edge to contact distance.

44. A device and/or assembly and/or method of production substantially as hereinbefore described with reference to any of the accompanying drawings.

The Patent Office

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Application No: GB 9621747.6
Claims searched: 1-10, 42, & 43

Examiner: SJ Morgan
Date of search: 9 January 1997

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KECB,KECX,KPAC)

Int Cl (Ed.6): H01L; G01T 1/24

Other: Online:WPI,JAPIO,INSPEC

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0 657 938 A1	(MINNESOTA MINING) See line 48 column 9 - line 51 column 10	1
X	US 4 467 342	(RCA) See lines 23-60, column 3	1, 6-9, & 42

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.